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History.SchDoc

Revision History

Rev.	Rel.	Date	Author	Description	Page(s)
1.1.1	RC00	2021-09-14	RP	- Initial design	
2	RC00	2023-8-9	GLS	Clean Up	
3	RC00	2024-4-22	JH	Finishing touches	

EVAL1_BUP_15N(06N)

EVAL1_BUP_06N

2

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IRHIR PSS HiRel M TM

Andover, Ma

04/2024

Link to Top Level Document

02 Top Level
Top_Level.SchDoc

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Title	EVAL1_BUP_15N(06N)		
Variant	EVAL1_BUP_06N	Approved	<Appr.>
Size: A3	Document Name: History.SchDoc	Rel.: JH	Rev.: 2
Author: Jack Heun			
Date: 8/29/2024 Time: 9:47:25 AM	SVN Revision: Not in version control		
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Top_Level.SchDoc

Schematic
Schematic.SchDoc

Gate Drivers, Half Bridge Power Stage

Miscellaneous
Miscellaneous.SchDoc

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Variant	EVAL1_BUP_06N	Approved	<Appr.>
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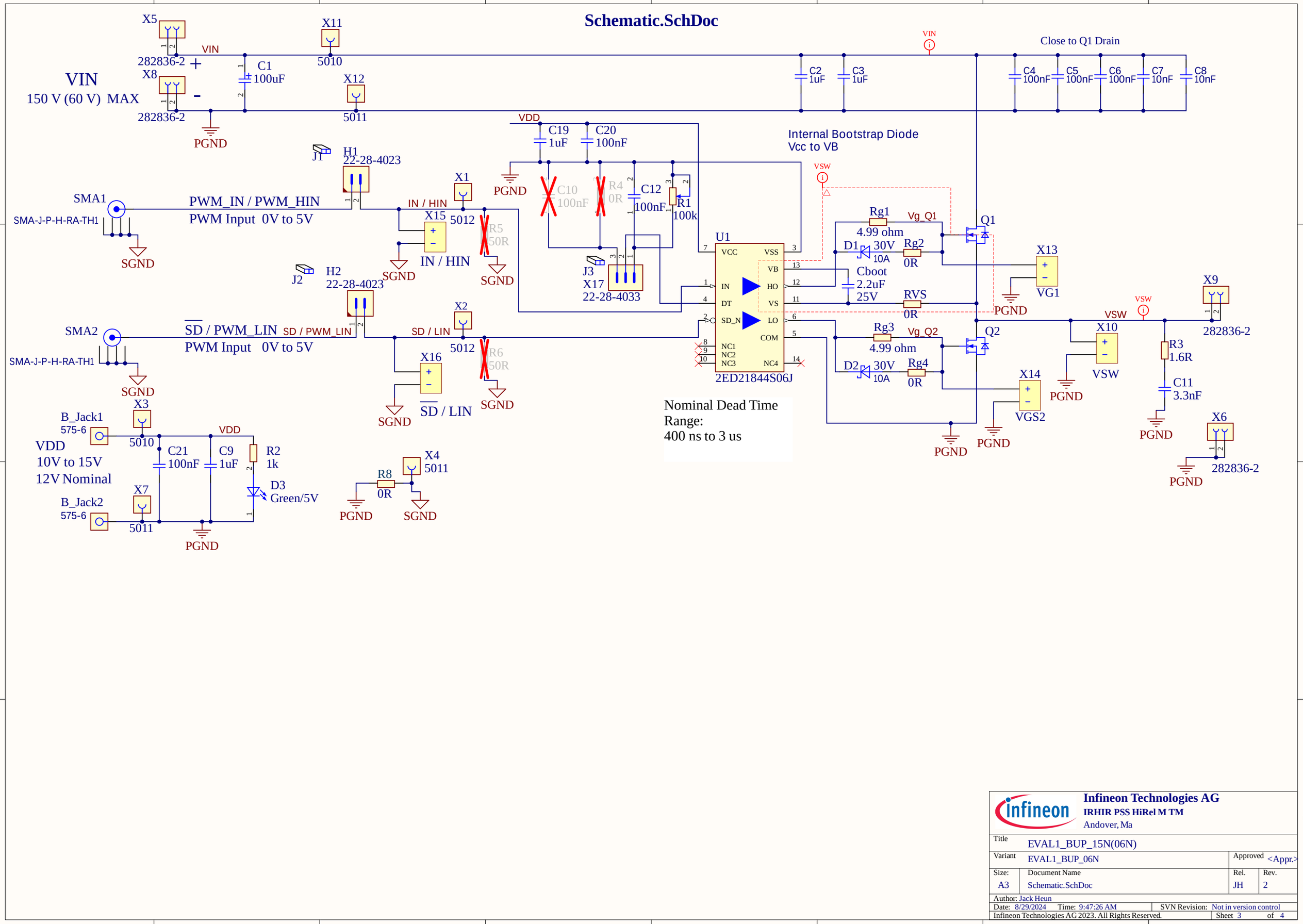

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Title	EVAL1_BUP_15N(06N)		
Variant	EVAL1_BUP_06N	Approved	<Appr.>
Size: A3	Document Name: Schematic.SchDoc	Rel. JH	Rev. 2
Author: Jack Heun			
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Miscellaneous.SchDoc

MP1



9434

MP2



9434

MP3



9434

MP4



9434

Fiducial Markers

E1



E2



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Title	EVAL1_BUP_15N(06N)		
Variant	EVAL1_BUP_06N	Approved	<Appr.>
Size: A3	Document Name: Miscellaneous.SchDoc	Rel.: JH	Rev.: 2

Author: Jack Heun
Date: 8/29/2024 Time: 9:47:26 AM SVN Revision: Not in version control

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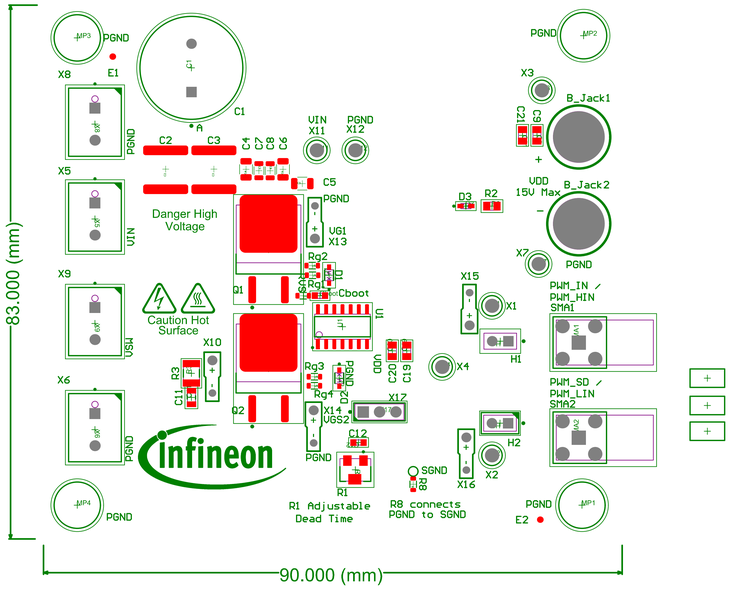
Layer	Name	Material	Thickness	Constant	Board Layer Stack
	Top Overlay				
	Top Solder	Solder Resist	0.40mil	3.5	
1	Layer 1	CF-005	2.76mil		
	Dielectric 1	FR-4	10.00mil	4.2	
2	Layer 2	CF-004	2.76mil		
	Dielectric 2	FR-4	30.18mil	4.2	
3	Layer 3	CF-004	2.76mil		
	Dielectric 3	FR-4	10.00mil	4.2	
4	Layer 4	CF-005	2.76mil		
	Bottom Solder	Solder Resist	0.40mil	3.5	
	Bottom Overlay				

Total board thickness: 62.00mil



DESIGN INFORMATION

MIN. TRACK WIDTH: 8 MIL
MIN. CLEARANCE: 0.12 mm
MIN. VIA PAD SIZE: 24 MIL
MINIMUM ANNULAR RING 0.05mm (2MIL) EXTERNAL
PER IPC-D-275 CLASS 2 LEVEL C
REGISTRATION TOLERANCES: METAL +/- 5 MIL, HOLES +/- 3 MIL
HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

MATERIAL:
[ ] FR-408 [X] FR-4 High Tg [ ] OTHER
THICKNESS: [X] 65 MIL (1.65mm) +/-10% [ ] OTHER
TOLERANCE: [X] ANSI IPC-6012 TYPE 3 CLASS 2 [ ] OTHER +/-
BOW & TWIST: [X] ANSI IPC-6012 TYPE 3 CLASS 2 [ ] OTHER +/-

DRILLING:
REFERENCE: [X] AS SHOWN [X] NC_DRILL FILES
PTH COPPER THICKNESS: [X] 20-30 um [ ] OTHER

BOARD FINISH:
SILKSCREEN: [X] TOP [X] BOTTOM
SILKSCREEN COLOR: [X] WHITE [ ] OTHER
SOLDER RESIST COLOR: [X] GREEN [ ] OTHER
[X] MATTE [ ] SEMI-GLOSS
SURFACE FINISH: [X] IMMERSION GOLD (ENIG) [ ] ENEPIG
[ ] IMM. TIN/SILVER OR EQUIV [ ] OTHER

ARRAY/PANEL: [ ] CUT AND TRIM PER M1 BOARD OUTLINE
[ ] N.C. ROUTE [X] V. SCORE

CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBS TO MEET OR EXCEED THE REQUIREMENTS OF:
[X] ANSI IPC-A-600F CLASS --> [ ] 1 [X] 2 [ ] 3
[X] RoHS [ ] OTHER PER ORDER

ALL BOARDS MUST MEET OR EXCEED UL94-VO REQUIREMENTS.
PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

ADDITIONAL REQUIREMENTS:
MICROSECTION: [ ] YES
BARE BOARD ELEC. TEST: [ ] NONE [X] REQUIRED [ ] PER ORDER

IOR HiRel
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Infineon Technologies AG
IRHR PSS HiRel M TM
101 N Pacific Coast Highway
El Segundo, CA 90245

ENGINEER:	TITLE: EVAL1_BUP_15N(06N)		
PCB DESIGNER: Jack Heun			
DATE: 8/29/2024	PART NO.:	REL: 2	REV: 2
SVN REVISION: Not in version control	FILE NAME: EVAL1_BUP_15N(06N).PcbDoc	APRV: JH	SCALE: 1:1

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TOR Hirel An Infineon Technologies Company Infineon Technologies AC IRHIR PSS HiRel M TM 101 N Pacific Coast Highway El Segundo, CA 90245	Not in version control SVN REVISION:	EVAL1_BUP_1SN(OSN)PcPDoc FILE NAME:	1H APRV:	1:1 SCALE:
	8\29\2024 DATE:	PART NO.:	2 REF:	2 REV:
	Jack Heun PCB DESIGNER:	EVAL1_BUP_1SN(OSN) TITLE:		
	ENGINEER:			

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